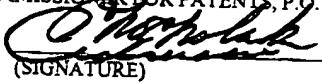


#15
RCE7/21/03 ~~7/16/03~~
AOPATENT APPLICATION
Docket No. 9903-045
Client No. S01US021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF MAILING UNDER 37 CFR 1.8

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE WITH SUFFICIENT POSTAGE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO MAIL STOP RCE, COMMISSIONER FOR PATENTS, P.O. BOX. 1450, ALEXANDRIA, VA. 22313-1450 ON JULY 16, 2003.
ADRIENNE CHOCHOLAK
(SENDER'S PRINTED NAME)


(SIGNATURE)

In re application of: Sung-Ho Ahn and Se-Yong Oh

Serial No. 10/008,704 Examiner: Tran, Tan N.

Confirmation No. 8392

Filed: December 6, 2001 Group Art Unit: 2826

For: ULTRA-THIN SEMICONDUCTOR PACKAGE DEVICE AND
METHOD FOR MANUFACTURING THE SAME

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

1. Submission required under 37 C.F.R. § 1.114

a. Previously submitted: Consider the amendment(s) reply under 37 C.F.R. § 1.116 previously filed on _____. Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____. Other:b. Enclosed is: Amendment/Reply

FAX RECEIVED

 Affidavit(s)/Declaration(s)

OCT 15 2003

 Information Disclosure Statement (IDS)

TECHNOLOGY CENTER 2000

2. Miscellaneous

Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; fee under 37 C.F.R. § 1.17(i) required).

3. Fees: (Note: The RCE fee under 37 C.F.R. §1.17(e) is required by 37 C.F.R. §1.114 when the RCE is filed)

RCE fee required under 37 C.F.R. § 1.17(e)

\$375 small entity
 \$750 large entity

Extension of time fee (37 C.F.R. §§1.136 and 1.17)

	small entity	large entity
<input checked="" type="checkbox"/> Extension of Time - 1 st	<input type="checkbox"/> \$55	<input checked="" type="checkbox"/> \$110
<input type="checkbox"/> Extension of Time - 2 nd	<input type="checkbox"/> \$205	<input type="checkbox"/> \$410
<input type="checkbox"/> Extension of Time - 3 rd	<input type="checkbox"/> \$465	<input type="checkbox"/> \$930

Suspension of application fee (37 C.F.R. § 1.17(i))-\$130

PTO Form 2038 authorizing credit card payment of \$860.00 filing fee (\$750.00) and extension fee (\$110.00) is enclosed.

Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.



20575
PATENT TRADEMARK OFFICE

Respectfully submitted,

MARGER JOHNSON & McCOLLUM, P.C.



Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLUM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

FAX RECEIVED

OCT 16 2003

TEC

PATENT APPLICATION
Docket No. 9903-045
Client No. S01US021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sung-Ho Ahn and Se-Yong Oh IN
Serial No. 10/008,704 Examiner: Tran, Tan N.
Confirmation No. 8392
Filed: December 6, 2001 Group Art Unit: 2826
For: ULTRA-THIN SEMICONDUCTOR PACKAGE DEVICE AND
METHOD FOR MANUFACTURING THE SAME

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION UNDER 37 CFR 1.114

A reply responsive to the Final Office Action, paper No. 11, dated March 20, 2003 ('Final Action'), was filed on May 22, 2003. The Examiner indicated in the Advisory Action dated June 9, 2003 ('Advisory Action') that the response failed to place the application in condition for allowance. Therefore, for purposes of this RCE, it is assumed that the amendments offered on May 22, 2003 were not entered. Responsive to the Final Action, please amend the above-identified application as follows.

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 16 of this paper.

FAX RECEIVED

OCT 16 2003

TECHNOLOGY CENTER 2800

MARGER JOHNSON & McCOLLOM
PROFESSIONAL CORPORATION

PATENT, TRADEMARK AND COPYRIGHT LAW,
TECHNOLOGY LICENSING & LITIGATION

1030 SW MORRISON STREET
PORTLAND, OREGON 97205 USA

(503) 222-3613
FAX: (503) 274-4622

Email: info@techlaw.com
Internet: www.techlaw.com

TO: Examiner Tan N. Tran, USPTO, Group Art Unit 2826
FAX: 703-308-7722
FROM: Todd Iverson
DATE: October 15, 2003
RE: Application Ser. No. 10/008,704, Attorney Docket No. 9903-045

Number of pages (including this one):

In case of error in transmission, call: 503-276-4815 (direct line)

REMARKS:

Dear Examiner Tran:

In our discussion earlier today, we agreed that the Advisory Action mailed on October 3, 2003 was incorrectly labeled with the wrong application serial number and attorney docket number. In other words, the Advisory Action that issued for this case was intended for another case altogether.

Per your request, please find enclosed a copy of the RCE that was filed for this case on July 16, 2003, using Express Mail Procedure. Your assistance in removing the improper Advisory Action from the file wrapper and correcting the PAIR system is appreciated.

If we may provide any other material that will assist you in this process, please do not hesitate to let me know.

Sincerely,


Todd Iverson, Reg. No. 53,057

NOTICE

This facsimile transmission is attorney-client privileged and confidential information intended only for the recipient named above. If you are not the intended recipient, you are hereby notified that any dissemination, distribution, use or copying of this communication is strictly prohibited. If you have received this transmission in error, contact us immediately at the number above.

FAX RECEIVED

OCT 15 2003

TECHNOLOGY CENTER 2800

This listing of claims will replace all prior versions, and listings, of claims in this application.

Listing of Claims

Claims 1-19 (Cancelled)

20. (Previously Amended) An ultra-thin semiconductor package device comprising:
a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie
bar connected to the die pad, said die pad including a chip attaching part having a first thickness
and a peripheral part surrounding and protruding away from the chip attaching part;
first and second semiconductor chips each including a plurality of electrode pads, wherein
the first semiconductor chip is bonded to a top surface of the chip attaching part and the second
semiconductor chip is bonded to a bottom surface of the chip attaching part;
a package body encapsulating the semiconductor chips; and
bonding wires configured to electrically connect the plurality of electrode pads and the
leads, said leads having inner leads encapsulated with the package body to which the bonding
wires are bonded and outer leads exposed from the package body, wherein the inner leads having
a second thickness, wherein the first thickness is smaller than the second thickness, wherein the
peripheral part has a thickness equal to the second thickness of the inner leads, and wherein the
peripheral part protrudes toward the second semiconductor chip.

21. (Original) An ultra-thin semiconductor package device according to claim 20,
wherein the die pad is disposed below the leads.

22. (Previously Amended) An ultra-thin semiconductor package device comprising:
a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie
bar connected to the die pad, said die pad including a chip attaching part having a first thickness
and a peripheral part surrounding and protruding away from the chip attaching part;
first and second semiconductor chips each including a plurality of electrode pads, wherein
the first semiconductor chip is bonded to a top surface of the chip attaching part and the second
semiconductor chip is bonded to a bottom surface of the chip attaching part;
a package body encapsulating the semiconductor chips; and
bonding wires configured to electrically connect the plurality of electrode pads and the
leads, said leads having inner leads encapsulated with the package body to which the bonding

wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and wherein the bonding wires connected to one of the semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip.

23. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein the bonding wires are connected by balls formed on the leads and stitches formed on the electrode pads.

24. (Original) An ultra-thin semiconductor package device according to claim 23, wherein metal bumps are formed on the electrode pads and wherein the stitches are formed on the metal bumps.

25. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein the die pad comprises divided first and second die pads.

26. (Original) An ultra-thin semiconductor package device according to claim 25, wherein the first and second die pads each include a corresponding chip attaching part and a corresponding peripheral part.

27. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

28. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein a thickness of the package body is about 580 μm , a thickness of the die pad peripheral part is about 100 μm , and a thickness of the chip attaching part is about 40 μm .

29. (Previously Amended) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

Claims 30-49 (withdrawn)

50. (Original) An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, wherein said die pad includes a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip having a plurality of electrode pads formed on an active surface of the chip, said chip connected to the chip attaching part;

a package body for encapsulating the semiconductor chip;

bonding wires encapsulated by the package body, said bonding wires configured to electrically connect the electrode pads of the semiconductor chip to the leads, wherein each of the plurality of leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body; and

wherein the chip attaching part has a first thickness and the inner lead has a second thickness that is greater than the first thickness.

51. (Original) An electronic apparatus according to claim 50, wherein the electronic apparatus is a memory card.

52. (Original) An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, said die pad including a chip attaching part and a peripheral part surrounding the chip attaching part, said peripheral part protruding away from the chip attaching part;

first and second semiconductor chips each having a plurality of electrode pads formed on an active surface of the chip, said first chip being attached to a top surface of the chip attaching part and the second chip being attached to a bottom surface of the chip attaching part;

a package body for encapsulating the semiconductor chip; and

bonding wires encapsulated by the package body and configured to electrically connect the electrode pads of the semiconductor chip and the plurality of leads, wherein each of the plurality of leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body,

wherein said chip attaching part has a first thickness and the inner lead has a second thickness greater than the first thickness and equal to a thickness of the peripheral part.

53. (Original) An electronic apparatus according to claim 52, wherein the electronic apparatus is a memory card.

54. (Currently amended) The ultra-thin semiconductor package device according to claim 44 52, further comprising another semiconductor chip attached to a back side of the chip attaching part.

55. (Currently Amended) An ultra-thin semiconductor package device comprising: a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads totally having a constant second thickness greater than the first thickness, wherein the chip attaching part and the peripheral part have the same thickness.

56. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein the inner leads are formed of a single layer.

57. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein the first thickness is between about 30% to 50% of the second thickness.

58. (Previously added) The ultra-thin semiconductor package device according to claim 55, further comprising another semiconductor chip attached to a back side of the chip attaching part.

59. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein the die pad is located below the leads.

60. (Previously added) The ultra-thin semiconductor package according to claim 55, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

61. (Previously added) The ultra-thin semiconductor package device according to claim 60, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

62. (Previously added) The ultra-thin semiconductor package device according to claim 55, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

63. (Previously Added) The ultra-thin semiconductor package device according to claim 59, wherein the tie bar has the same thickness as the leads.

64. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the tie bar has the same thickness as the die pad peripheral part.

65. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

66. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the die pad comprises divided first and second die pads.

67. (Previously Added) The ultra-thin semiconductor package device according to claim 66, wherein the first and second die pads each include a chip attaching part and a peripheral part.

68. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

69. (Previously Added) The ultra-thin semiconductor package device according to claim 60, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

70. (Previously Added) The ultra-thin semiconductor package device according to claim 55, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

71. (Currently Amended) An ultra-thin semiconductor package device comprising: a lead frame comprising a die pad, a plurality of leads disposed around the die pad, wherein each of the plurality of leads comprises an inner lead and an outer lead, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein each of the plurality of electrode pads is electrically connected to at least one of the plurality of leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and a portion of the inner leads having a second thickness greater than the first thickness, wherein the bonding wires are directly connected to the portion of the inner leads, and wherein the chip attaching part and the peripheral part have the same thickness.

72. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the inner leads are formed of a single layer.

73. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the first thickness is between about 30% to 50% of the second thickness.

74. (Previously Added) The ultra-thin semiconductor package device according to claim 71, further comprising another semiconductor chip attached to a back side of the chip attaching part.

75. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the die pad is located below the leads.

76. (Previously Added) The ultra-thin semiconductor package according to claim 71, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

77. (Previously Added) The ultra-thin semiconductor package device according to claim 76, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

78. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

79. (Previously Added) The ultra-thin semiconductor package device according to claim 75, wherein the tie bar has the same thickness as the leads.

80. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the tie bar has the same thickness as the die pad peripheral part.

81. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

82. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the die pad comprises divided first and second die pads.

83. (Previously Added) The ultra-thin semiconductor package device according to claim 82, wherein the first and second die pads each include a chip attaching part and a peripheral part.

84. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

85. (Previously Added) The ultra-thin semiconductor package device according to claim 76, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

86. (Previously Added) The ultra-thin semiconductor package device according to claim 71, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

87. (Previously Added) An ultra-thin semiconductor package device comprising:
a lead frame having a die pad, a plurality of leads disposed around the die pad, and tie bars connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding the chip attaching part;

a first and a second semiconductor chip each including a plurality of electrode pads connected to the leads by bonding wires, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part; and

a package body encapsulating the first and the second semiconductor chips;
wherein said leads have a plurality of inner leads to which the bonding wires are bonded encapsulated within the package body, wherein said leads have a plurality of outer leads exposed from the package body, wherein the plurality of inner leads have a second thickness that is greater than the first thickness, and wherein the bonding wires connected to one of the first and the second semiconductor chips are shorter than the bonding wires connected to the other one of the first and the second semiconductor chips.

88. (Previously Added) The ultra-thin semiconductor package device according to claim 87, wherein the peripheral part protrudes upwards and away from the chip attaching part, and wherein the bonding wires connected to an upper one of the first and the second semiconductor chips are shorter than the bonding wires connected to a lower one of the first and the second semiconductor chips.

89. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the inner leads are formed of a single layer.

90. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the first thickness is between about 30% to 50% of the second thickness.

91. (Previously Added) The ultra-thin semiconductor package according to claim 88, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

92. (Previously Added) The ultra-thin semiconductor package device according to claim 91, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

93. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

94. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the tie bars have the same thickness as the leads.

95. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the tie bars have the same thickness as the peripheral part.

96. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

97. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the die pad comprises divided first and second die pads.

98. (Previously Added) The ultra-thin semiconductor package device according to claim 97, wherein the first and second die pads each include a chip attaching part and a peripheral part.

99. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

100. (Previously Added) The ultra-thin semiconductor package device according to claim 99, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

101. (Previously Added) The ultra-thin semiconductor package device according to claim 88, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

102. (Previously Added) The ultra-thin semiconductor package device according to claim 87, wherein the peripheral part protrudes downwards and away from the chip attaching part, and wherein the bonding wires connected to a lower one of the first and the second semiconductor chips are shorter than the bonding wires connected to an upper one of the first and the second semiconductor chips.

103. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the inner leads are formed of a single layer.

104. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the first thickness is between about 30% to 50% of the second thickness.

105. (Previously Added) The ultra-thin semiconductor package according to claim 102, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

106. (Previously Added) The ultra-thin semiconductor package device according to claim 105, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

107. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

108. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the tie bars have the same thickness as the leads.

109. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the tie bars have the same thickness as the peripheral part.

110. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

111. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the die pad comprises divided first and second die pads.

112. (Previously Added) The ultra-thin semiconductor package device according to claim 111, wherein the first and second die pads each include a chip attaching part and a peripheral part.

113. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

114. (Previously Added) The ultra-thin semiconductor package device according to claim 113, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

115. (Previously Added) The ultra-thin semiconductor package device according to claim 102, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

116. (New) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part and another semiconductor chip mounted to another side of the chip attaching part, said semiconductor chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a second thickness greater than the first thickness.

117. (New) An ultra-thin semiconductor package device according to claim 116, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

118. (New) The semiconductor package device of claim 50, wherein the first thickness is between about 30% to 50% of the second thickness.

119. (New) The semiconductor package device of claim 50, wherein the chip attaching part and the peripheral part have the same thickness.

120. (New) The semiconductor package device of claim 50 further comprising another semiconductor chip attached to a back side of the chip attaching part.

121. (New) The semiconductor package device of claim 50, wherein the die pad is located below the leads.

122. (New) The semiconductor package of claim 50, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

123. (New) The semiconductor package device of claim 122, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

124. (New) The semiconductor package device of claim 50, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

125. (New) The semiconductor package device of claim 121, wherein the tie bar has the same thickness as the leads.

126. (New) The semiconductor package device of claim 50, wherein the tie bar has the same thickness as the die pad peripheral part.

127. (New) The semiconductor package device of claim 50, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

128. (New) The semiconductor package device of claim 50, wherein the die pad comprises divided first and second die pads.

129. (New) The semiconductor package of claim 128, wherein the first and second die pads each include a chip attaching part and a peripheral part.

130. (New) The semiconductor package device of claim 50, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

131. (New) The semiconductor package device of claim 122, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

132. (New) The semiconductor package device of claim 50, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

133. (New) The ultra-thin semiconductor package device of claim 58, wherein the semiconductor chip and the another semiconductor chip are of the same type.

134. (New) The ultra-thin semiconductor package device of claim 74, wherein the semiconductor chip and the another semiconductor chip are of the same type.

135. (New) The ultra-thin semiconductor package device of claim 116, wherein the peripheral part protrudes from only one side of the chip attaching part.

136. (New) The ultra-thin semiconductor package device of claim 116, wherein the peripheral part protrudes upward from the chip attaching part.

137. (New) An ultra-thin semiconductor package device comprising:
a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;
at least one semiconductor chip, the at least one semiconductor chip including a plurality of electrode pads, wherein the at least one semiconductor chip is bonded to a surface of the chip attaching part;
a package body encapsulating the at least one semiconductor chip; and
bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads have a second thickness, wherein the first thickness is smaller than the second thickness, and wherein the peripheral part only protrudes downward.

138. (New) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a top surface of the chip attaching part.

139. (New) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a bottom surface of the chip attaching part.

140. (New) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a top surface of the chip attaching part, and wherein at least one other semiconductor chip is attached to a bottom surface of the chip attaching part.

141. (New) The ultra-thin semiconductor package device of claim 137, wherein the peripheral part has a thickness equal to the second thickness.

REMARKS

Claims 30-49 were withdrawn.

Claims 20-29, 50-53, and 87-115 stand allowed.

Claims 1-3, 5-10, 12-16, and 55-86 stand rejected.

Claims 4, 11, 54, 58, 65, 74 and 81 stand objected to.

Claims 1-19 are cancelled.

In accordance with the Examiner's suggestions, claims 54, 55, and 71 are amended. No new subject matter is present in these claims.

New claims 116-141 are added. No new subject matter is present in these claims.

Claims 20-29 and 50-117 are pending. Claims 20-29, 50-53, and 87-115 are allowed.

The applicant submits that the remaining pending claims 54-86 and 116-141 are allowable and such allowance is respectfully requested in light of the following remarks.

35 USC §112 Rejections

Claims 55-70 and 72 stand rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

According to the Examiner, the specification does not disclose the inner leads having a constant second thickness as recited in claim 55 (emphasis in original). The applicant disagrees. To the contrary, the application as originally filed teaches that the leads are of two portions, inner leads (116a of FIG. 3a) that are within the package body, and outer leads (116b of FIG. 3a) that are located outside the package body (page 7, lines 30-34). FIG. 3a clearly shows that the inner leads 116a (everything within the package body) are of a constant second thickness, as recited in claim 55. Applicant notes that the recited first thickness of claim 55 is in reference to the recited chip attaching part and recited peripheral part (112a and 112b of FIG. 3a).

According to the Examiner, the specification does not disclose the inner leads are formed of a single layer as recited in claims 56 and 72 (emphasis in original). The applicant disagrees. FIG. 3a clearly shows that the leads 116 (inner leads 116a and outer leads 116b) have only a single layer, represented by the cross-hatching within the leads 116, indicating a single layer. This would be apparent to one of ordinary skill in the art.

The applicants submit that these rejections are overcome.

35 USC §102 Rejections

Claims 1-3, 5, 8-10, 55, 57, 59, 62-64, 71, 73, 75, and 78-80 stand rejected under 35 USC §102(b) as being anticipated by US Patent No. 5,014,113 issued to Casto, et al. (Casto). The applicant disagrees for the following reasons.

Claims 1-3, 5, and 8-10 are cancelled.

With regard to claim 55, in the Advisory Action the Examiner suggested that if the claim was amended to recite inner leads "totally" having a constant second thickness, the claim would distinguish over the Casto reference. The applicants adopt the Examiner's suggestion and amend claim 55 in this manner.

The applicant submits that claims 56-70 are allowable for at least the same reason as claim 55.

With regard to claim 71, in the Advisory Action the Examiner suggested that if the claim was amended to recite bonding wires "directly connected" to the portion of the inner leads, the claim would distinguish over the Casto reference. The applicants adopt the Examiner's suggestion and amend claim 71 in this manner.

The applicant submits that claims 72-86 are allowable for at least the same reason as claim 71.

35 USC §103 Rejections

Claims 6, 7, 16, 60, 61, 76, 77, 70 and 86 stand rejected under 35 USC §103(a) as being unpatentable over Casto.

Claims 6, 7, and 16 are cancelled. Claims 60, 61, 70, 76, 77, and 86 are dependent upon either claim 55 or 71. The applicants have amended claims 55 and 71 in a manner suggested by the Examiner to distinguish over the Casto reference. Thus, claims 60, 61, 70, 76, 77, and 86 are patentable over Casto because Casto fails to establish a *prima facie* case of obviousness with respect to them.

Claims 12-14, 66-68 and 82-84 stand rejected under 35 USC 103(a) as being unpatentable over Casto in view of Huang (2002/0113305).

Claims 12-14 are cancelled. Claims 66-68 and 82-84 are dependent upon either claim 55 or 71. The applicants have amended claim 55 and 71 in a manner suggested by the Examiner to distinguish over the Casto reference. The Huang reference also fails to disclose the elements of claims 55 and 71 that Casto lacks. Thus, a *prima facie* case of obviousness is not established with respect to claims 66-68 and 82-84 because the Casto/Huang combination fails to disclose all limitations inherent to claims 66-68 and 82-84. Consequently, claims 66-68 and 82-84 are allowable for at least the same reasons as claims 55 and 71, respectively.

Claims 15, 69 and 85 stand rejected under 35 USC §103(a) as being unpatentable over Casto in view of Kozono (6,177,718).

Claim 15 is cancelled. Claims 69 and 85 are dependent upon claim 55 and 71, respectively. The applicant have amended claims 55 and 71 in manner suggested by the Examiner to distinguish over the Casto reference. Kozono also fails to disclose the elements of claims 55 and 71 that Casto lacks. Thus, a *prima facie* case of obviousness is not established with respect to claims 69 and 85 because the Casto/Kozono combination fails to disclose all limitations inherent to claims 69 and 85. Consequently, claims 69 and 85 are allowable for at least the same reasons as claims 55 and 71, respectively.

Allowable Subject Matter

Claims 20-29, 50-53, and 87-115 stand allowable over the prior art of record.

Claims 4, 11, 54, 58, 65, 74 and 81 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regard to claim 4, new claim 116 is added that contains all the limitations of claim 4 (claim 4 is henceforth cancelled) and its base claim (claim 1, which is henceforth cancelled).

With regard to claim 11, new claim 117 is added that contains all the limitations of claim 11 (claim 11 is henceforth cancelled), and claim 117 is made dependent upon allowable claim 116.

With regard to claim 54, the applicant notes that it contains the same limitation as original claim 4. Thus, it appears that when claim 54 was previously added it was mistakenly made to be dependent upon original claim 11 (original claim 11 was dependent upon original claim 4) rather than upon previously added claim 52. Since the Examiner has indicated claim 52 is allowable, claim 54 is amended to be dependent upon claim 52. The objection to claim 54 is overcome.

With regard to claims 58 and 65, they are dependent upon claim 55, which has been previously shown to be allowable. Consequently, the objections to these claims are overcome.

With regard to claims 74 and 81, they are dependent upon claim 71, which has been previously shown to be allowable. Consequently, the objections to these claims are overcome.

New Claims

As previously mentioned, new claim 116 and 117 were added to incorporate an otherwise allowable dependent claim into a rejected base claim.

New claims 118-132 are added that depend from allowed claim 50. No new subject matter is added, as the new claims are based upon cancelled claims 2-16.

New claim 133 is added that depends from claim 58, which the Examiner has indicated contains allowable subject matter. Claim 58 depends from claim 55. Claim 55 was previously shown to be allowable. No new subject matter is added. Support for the claim may be found, among other places, on page 11, lines 13-22

New claim 134 is added that depends from claim 74, which the Examiner has indicated contains allowable subject matter. Claim 74 depends from claim 71. Claim 71 was previously shown to be allowable. No new subject matter is added. Support for the claim may be found, among other places, on page 11, lines 13-22.

New claims 135-136 are added that depend from claim 116. No new subject matter is added.

New claims 137-141 are added. Claims 138-141 depend from claim 137. No new subject matter is added, as support for claim 137 is found in FIG. 10 and in claim 20.

Conclusion

For the foregoing reasons, allowance of claims 20-29 and 50-141 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

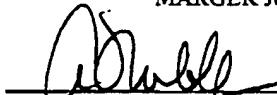


Respectfully submitted,

20575

PATENT TRADEMARK OFFICE
P.C.

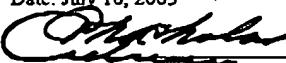
MARGER JOHNSON & McCOLLOM,



Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

I hereby certify that this correspondence
is being deposited with the United States
Postal Service as first class mail in an
envelope addressed to: Commissioner for
Patents, Washington, DC 20231
Date: July 16, 2003



Adrienne Chocholak

FAX RECEIVED

OCT 15 2003
TECHNOLOGY CENTER 2030